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(56) Documents Cited
US 6180490 B US 5943589 A US 5786262 A

(58) Field of Search
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INT CL[7] H01L 21/762
Online: WPI, EPODOC, JAPIO

(54) Abstract Title
Semiconductor device manufacturing method

(57) A manufacturing method for a semiconductor device includes forming a pad silicon oxide film 2 on a semiconductor substrate 1, forming a silicon nitride film 3 on the pad silicon oxide film, removing the silicon nitride film and the pad silicon oxide film respectively corresponding to a part in which a trench 1a is formed and exposing the semiconductor substrate, etching the exposed semiconductor substrate and forming the trench, forming an oxygen permeable oxide liner film 5 on the inner surface of the trench, and thermally oxidizing an area 1b of the semiconductor substrate via the oxide film.

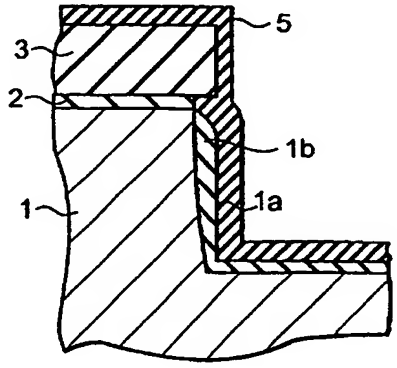

FIG.4

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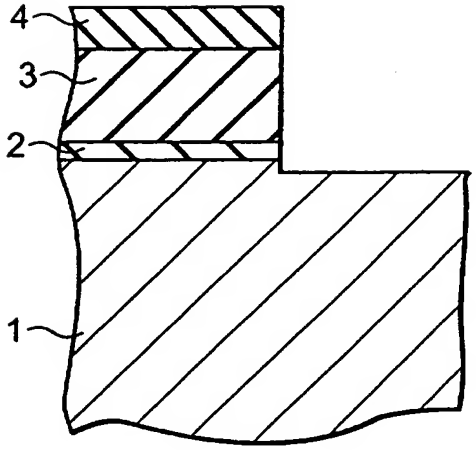

FIG.1

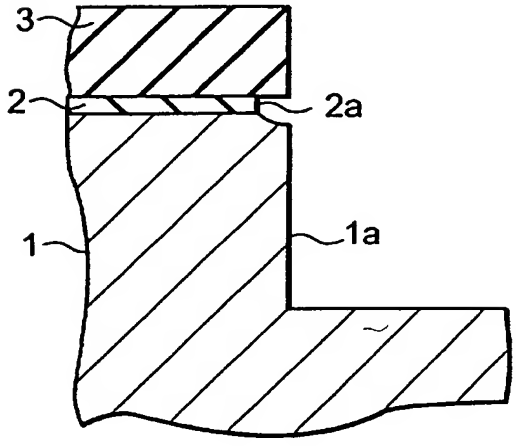

FIG.2

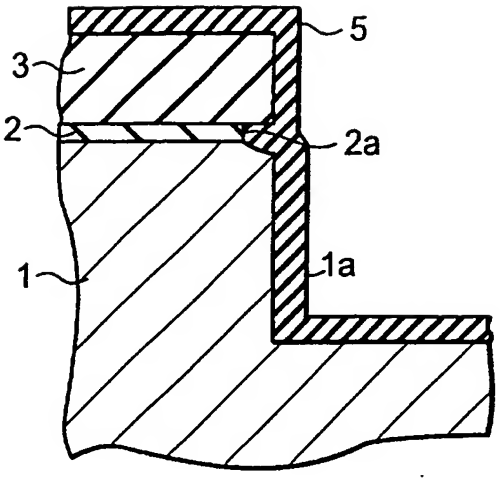

FIG.3

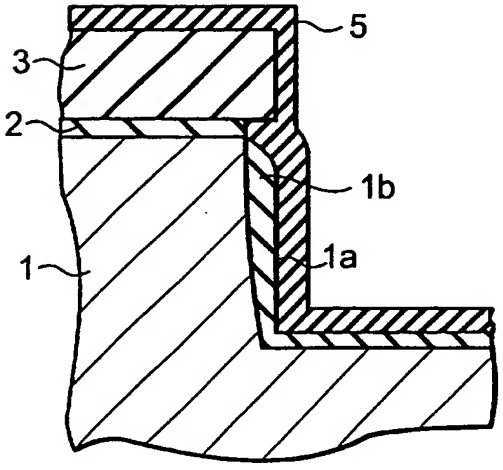

FIG.4

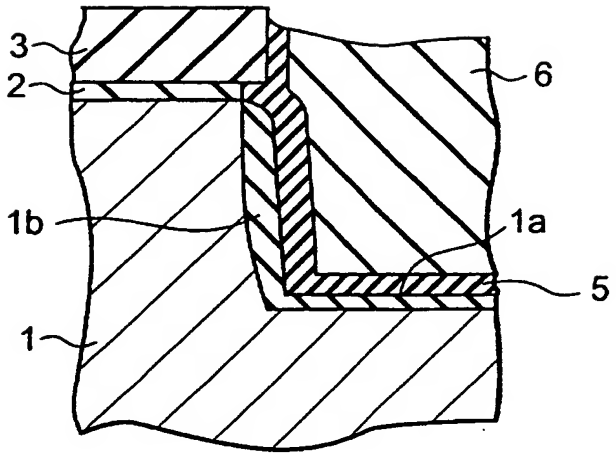

FIG.5

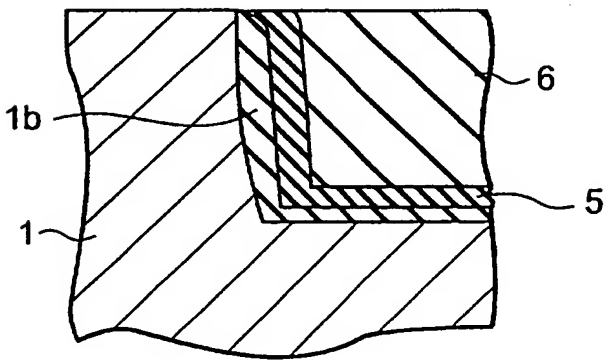

FIG.6

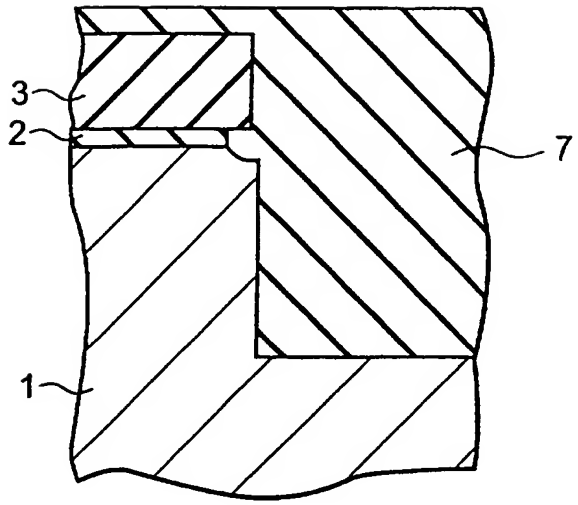

FIG.7

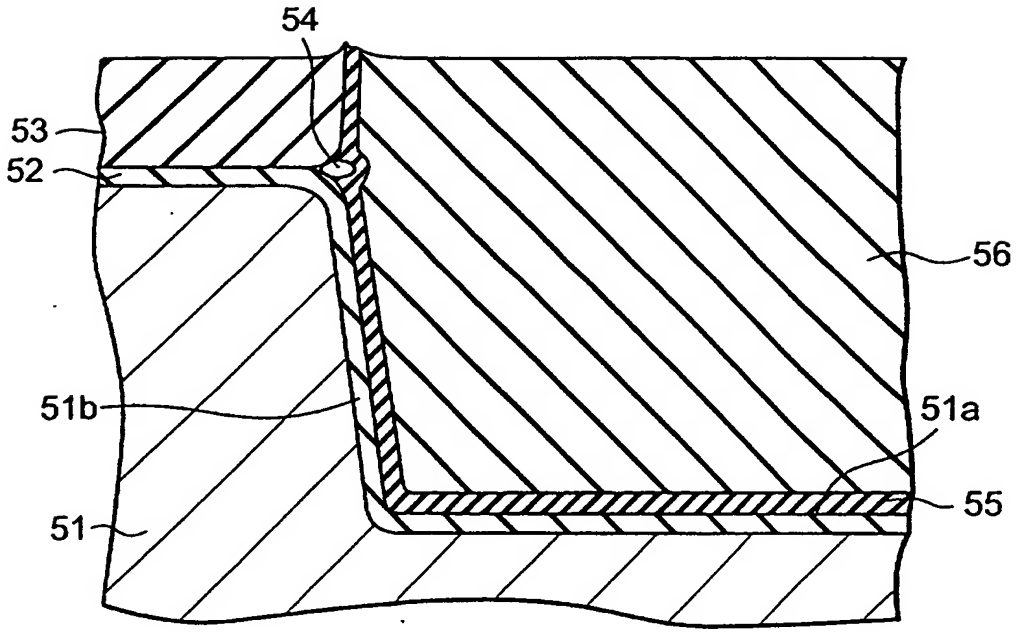

FIG.8

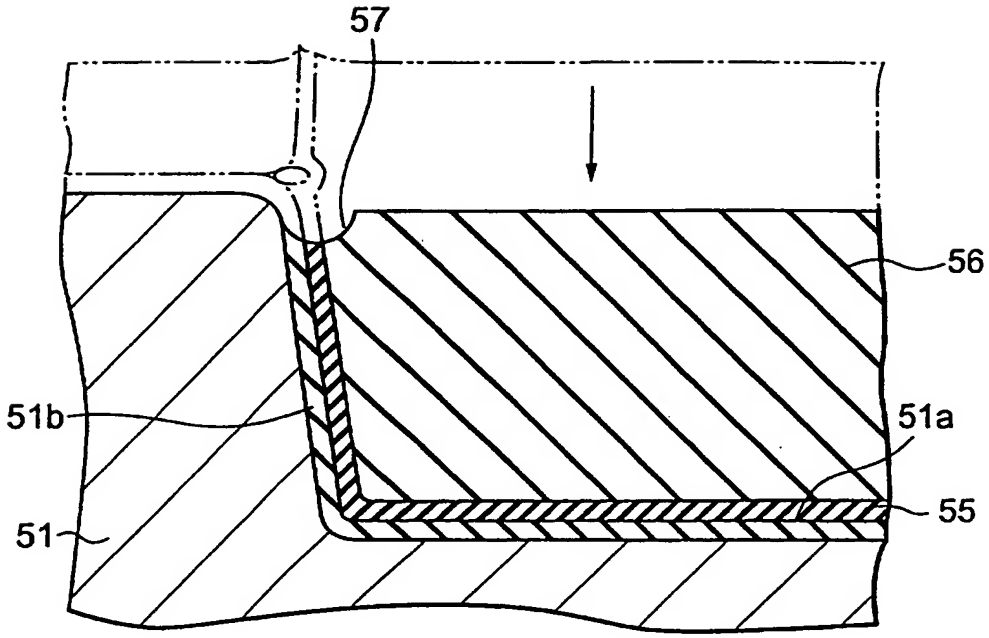

FIG.9

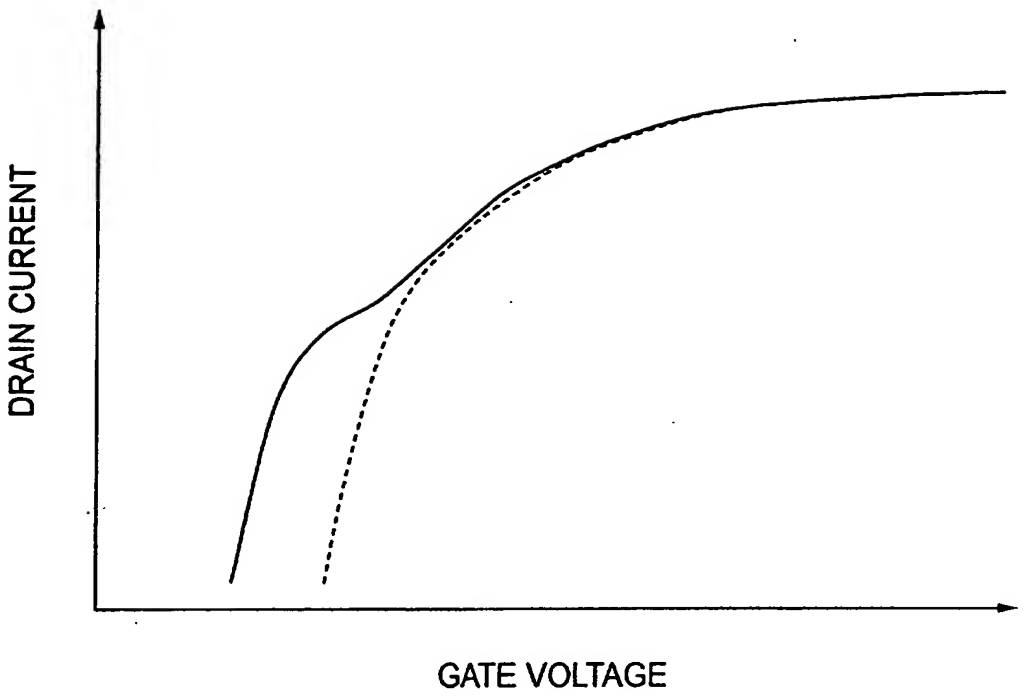

FIG.10

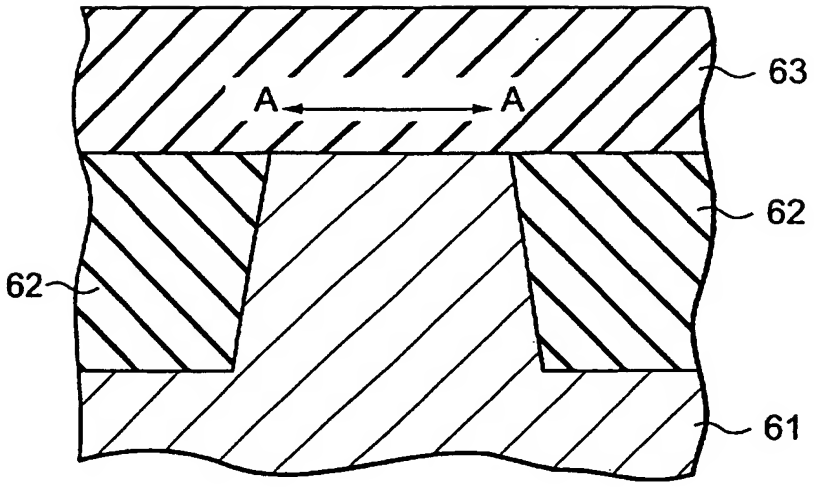

FIG.11A

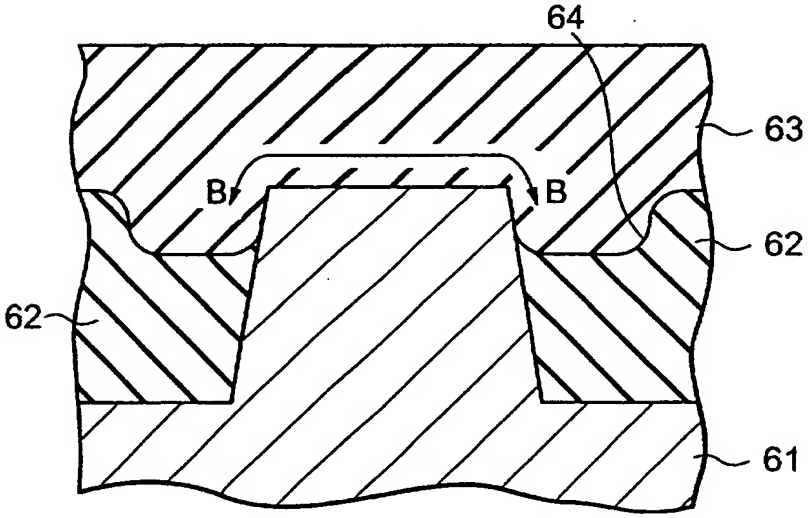

FIG.11B

SEMICONDUCTOR DEVICE MANUFACTURING METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the manufacturing method of a semiconductor device, particularly relates to the manufacturing method of a semiconductor device provided with trench isolation structure.

Description of the Prior Art

A process for isolating an element in the manufacturing method of a semiconductor device mainly has two ways of isolation by a trench and isolation by selective oxidation. FIGS. 8 and 9 are sectional views showing the manufacturing method of a semiconductor device adopting known type trench isolation in the order of a process.

In a known type manufacturing method, first, as shown in FIG. 8, a pad silicon oxide film 52 and a silicon nitride film 53 are sequentially formed on a flat silicon substrate 51. After resist is patterned, a trench 51a is formed on the silicon substrate 51 by plasma etching processing. Next, a thermal oxidation film 51b is formed on the exposed surface of the trench 51a of the silicon substrate 51. Afterward, a liner film 55 is formed on the overall surface. Next, a trench insulating film 56 made of high-density plasma oxide film is embedded in the trench 51a.

Afterward, the surface of the trench insulating film 56 is flattened as shown in FIG. 9 by suitably performing chemical mechanical polishing (CMP), oxide film etching and nitride film etching so that the height of the trench insulating film is equal to that of the surface of the silicon substrate 51.

Next, a semiconductor device is completed by forming a gate oxide film, a gate electrode (not shown) and others.

According to the known type manufacturing method of a semiconductor device, when the trench 51a is formed, a crystal defect is caused on the surface of the silicon substrate 51, however, such a crystal defect is eliminated by the formation of the thermal oxidation film 51. Also, as the liner film 55 functions as a buffer layer, stress that acts from the trench insulating film 56 which is a dense film onto the silicon substrate 51 is relieved.

Such a known type manufacturing method is disclosed in Japanese published unexamined patent applications No. Hei 8-46029 and No. Hei 11-176924 for example.

However, in the known type manufacturing method, as shown in FIG. 8, the end of the silicon nitride film 53 is pushed out by heating when the thermal oxidation film 51b is formed and a cavity 54 is formed between the silicon nitride film 53 and the pad silicon oxide film 52. Afterward, the oxide film is etched a few times, however, as in etching the oxide film, etching isotropically progresses, the cavity 54a is expanded to the trench insulating film 56 as shown in FIG. 9 and a concave portion 57 called a divot is formed in the trench

51a. When such a concave portion 57 exists in the trench 51a, there is a problem that the length of a channel is substantially longer than the design value and the characteristics vary.

FIG. 10 is a graph showing the characteristic of a bump of a transistor and showing gate voltage on its x-axis and drain current on its y-axis. In FIG. 10, a broken line shows the characteristics in design and a full line shows the characteristics of a semiconductor device in which a divot exists. As shown in FIG. 10, when a divot exists, the semiconductor device has characteristics that the part is turned on ahead and two steps of threshold voltage exist.

FIG. 11A is a schematic drawing showing a designed semiconductor device and FIG. 11B is a schematic drawing showing a semiconductor device manufactured according to a conventional type method. In FIGS. 11A and 11B, a gate oxide film and others are omitted for convenience.

As shown in FIG. 11A, in design, a trench insulating film 62 is formed on the surface of a silicon substrate 61, a gate electrode 63 is formed on them and a transistor having channel length shown by an arrow A-A is manufactured. However, according to the known type manufacturing method, as shown in FIG. 11B, as a divot 64 is formed, the channel length of the manufactured transistor is as shown by an arrow B-B. As described above, according to the conventional type manufacturing method, it is difficult to manufacture a transistor having channel length according to design.

In addition, as the shape of the divot is not fixed, the

degree of displacement off the characteristics varies every manufacture. Therefore, it is also extremely difficult to design in consideration of displacement due to a divot off the characteristics beforehand.

BRIEF SUMMARY OF THE INVENTION

The manufacturing method of a semiconductor device according to the invention includes a process for forming a pad silicon oxide film on a semiconductor substrate, a process for forming a silicon nitride film on the pad silicon oxide film, a process for removing the silicon nitride film and the pad silicon oxide film respectively corresponding to a part in which a trench is formed and exposing the semiconductor substrate, a process for etching the exposed semiconductor substrate and forming the trench, a process for forming an oxide film which an oxygen atom can pass at least on the inner surface of the

trench and a process for thermally oxidizing an area opposite to the trench of the semiconductor substrate via the oxide film.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other objects, features and advantages of this invention will become more apparent by reference to the following detailed description of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a sectional view showing the manufacturing method of a semiconductor device equivalent to a first embodiment of the invention;

FIG. 2 shows the first embodiment of the invention and is a sectional view showing the next process of a process shown in FIG. 1;

FIG. 3 shows the first embodiment of the invention and is a sectional view showing the next process of the process shown in FIG. 2;

FIG. 4 shows the first embodiment of the invention and is a sectional view showing the next process of the process shown in FIG. 3;

FIG. 5 shows the first embodiment of the invention and is a sectional view showing the next process of the process shown in FIG. 4;

FIG. 6 shows the first embodiment of the invention and is a sectional view showing the next process of the process shown

in FIG. 5;

FIG. 7 is a sectional view showing the manufacturing method of a semiconductor device equivalent to a second embodiment of the invention;

FIG. 8 is a sectional view showing the manufacturing method of a semiconductor device adopting known type trench isolation;

FIG. 9 shows a known type manufacturing method and is a sectional view showing the next process of the process shown in FIG. 8;

FIG. 10 is a graph showing the characteristics of a bump of a transistor; and

FIGS. 11A and 11B are schematic drawings showing a designed semiconductor device.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings, embodiments of the invention will be described below.

FIG. 1 is a plan showing an example of the layout of a semiconductor device equivalent to an embodiment of the invention. Referring to the attached drawings, the manufacturing method of the semiconductor device equivalent to the embodiment of the invention will be concretely described below. FIGS. 1 to 6 are sectional views showing the manufacturing method of the semiconductor device equivalent to the first embodiment of the invention in the order of a process.

In the first embodiment, first, as shown in FIG. 1, a pad

silicon oxide film 2 is formed on a silicon substrate 1. Next, a silicon nitride film 3 is formed on the pad silicon oxide film 2. Further, a high-temperature oxide film 4 is formed on the silicon nitride film 3. After resist formed on/over these is patterned, an opening is formed in an area in which isolation by a trench is performed is formed by plasma-etching the high-temperature oxide film 4, the silicon nitride film 3 and the pad silicon oxide film 2. At this time, the surface of the silicon substrate 1 is also slightly etched.

Next, after the corner of the silicon substrate 1 is rounded by Bronson processing, a trench 1a is formed on the silicon substrate 1 by plasma etching processing as shown in FIG. 2. Next, deposit generated in etching and others are removed by peeling by acid and the wet etching of the oxide film. At this time, as shown in FIG. 2, as the pad silicon oxide film 2 is also slightly etched, a cavity 2a is formed between the silicon nitride film 3 and the silicon substrate 1.

Afterward, acid cleaning is performed and as shown in FIG. 3, a liner film 5 is formed by a plasma-activated chemical vapor deposition method (plasma CVD). At this time, the liner film 5 invades into the cavity 2a. The liner film 5 is made of an oxide film such as a nonsilicate glass (NSG) film or a high-temperature oxide (HTO) film of tetraethyl orthosilicate (TEOS) for example and the thickness is 300 to 500 Å for example.

Next, an oxygen atom is made pass the liner film 5 and reaches the surface of the silicon substrate 1 by performing acid cleaning and thermal oxidation and as shown in FIG. 4, a

thermal oxidation film 1b is formed in a part in which the trench 1a of the silicon substrate 1 is formed.

Next, as shown in FIG. 5, a trench insulating film 6 made of a high-density plasma oxide film is embedded in the trench 1a. Afterward, flattening is made by CMP and next, the height of the trench insulating film 6 is reduced by wet etching. Next, as shown in FIG. 6, the silicon nitride film 3 and the pad silicon oxide film 2 are sequentially removed.

Afterward, the semiconductor device is completed by forming a gate oxide film, a gate electrode (not shown) and others.

As described above, in the first embodiment, as the surface of the trench 1a of the silicon substrate 1 is thermally oxidized via the liner film 5 after the linear film 5 is formed, the silicon nitride film 3 is surrounded by the liner film 5 in forming the thermal oxidation film 1b and even if the silicon nitride film 3 is heated, no lifting is caused. Therefore, as shown in FIG. 6, after the trench insulating film 6 is flattened, no divot also exists. Therefore, the characteristics of a device such as a transistor according to design can be acquired.

In the first embodiment, the high-density plasma oxide film is used for the trench insulating film 6, however, an oxide film formed by CVD may be also used. For the oxide film by CVD, a TEOS-NSG film or an HTO film may be also used for example.

Next, a second embodiment of the invention will be described. In the second embodiment, at the same time as the formation of a liner film, a trench insulating film is formed.

FIG. 7 is a sectional view showing the manufacturing method of a semiconductor device equivalent to the second embodiment of the invention. In the second embodiment shown in FIG. 7, the same reference number is allocated to the same component as that in the first embodiment shown in FIGS. 1 to 6 and the detailed description is omitted.

In the second embodiment, a process until before the liner film is formed (till the process shown in FIG. 2) is executed as a process similar to that in the first embodiment. Afterward, as shown in FIG. 7, a trench insulating film 7 is embedded in a trench 1a by CVD. That is, the linear film and the trench insulating film are collectively formed.

Next, an oxygen atom is made to reach the surface of the silicon substrate 1 via the trench insulating film 7 by thermal oxidation and a thermal oxidation film (not shown) is formed in a part in which the trench 1a of the silicon substrate 1 is formed.

Next, flattening is performed by CMP and next, the height of the trench insulating film 7 is reduced by wet etching. Next, the silicon nitride film 3 and the pad silicon oxide film 2 are sequentially removed.

Afterward, a semiconductor device is completed by forming a gate oxide film, a gate electrode (not shown) and others.

In the second embodiment, as in the first embodiment, a divot can be also prevented from being formed. Therefore, the characteristics of a device such as a transistor according to design can be acquired. Also, though time required for

oxidation is long because an oxide film covering the area is thick when the thermal oxidation film is formed, the number of processes can be reduced because the liner film and the trench insulating film are collectively formed.

In the second embodiment, for the trench insulating film 7, a TEOS-NSG film or an HTO film may be used for example.

As detailedly described above and illustrated, as an area opposite to the trench of the semiconductor substrate is thermally oxidized via an oxide film after the oxide film which an oxygen atom can pass is formed on the inner surface of the trench, the silicon nitride film can be prevented from being lifted in thermal oxidation even if the silicon nitride film is formed before these processes. Hereby, the formation of a divot in the succeeding etching of the oxide film can be prevented. Therefore, a transistor and others having stable characteristics can be manufactured.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments will become apparent to persons skilled in the art upon reference to the description of the invention.

CLAIMS

1. A manufacturing method of a semiconductor device, comprising:

a process for forming a trench on the surface of a semiconductor substrate;

a process for forming an oxide film which an oxygen atom can pass on the inner surface of the trench; and

a process for thermally oxidizing an area opposite to the trench of the semiconductor substrate via the oxide film.

2. A manufacturing method of a semiconductor device according to Claim 1, wherein:

said process for forming the oxide film is a process for forming a nonsilicate glass film of tetraethyl orthosilicate by a chemical vapor deposition method (CVD).

3. A manufacturing method of a semiconductor device according to Claim 1, wherein:

said process for forming the oxide film is a process for forming a high-temperature oxide film by CVD.

4. A manufacturing method of a semiconductor device according to Claim 1, wherein:

said process for forming the oxide film includes a process for embedding an oxide film in said trench.

5. A manufacturing method of a semiconductor device,

comprising:

a process for forming a pad silicon oxide film on a semiconductor substrate;

a process for forming a silicon nitride film on the pad silicon oxide film;

a process for removing the silicon nitride film and the pad silicon oxide film respectively corresponding to a part in which the trench is formed and exposing the semiconductor substrate;

a process for etching the exposed semiconductor substrate and forming a trench;

a process for forming an oxide film which an oxygen atom can pass at least on the inner surface of the trench; and

a process for thermally oxidizing an area opposite to the trench of the semiconductor substrate via the oxide film.

6. A manufacturing method of a semiconductor device according to Claim 5, wherein:

said process for forming the oxide film is a process for forming a nonsilicate glass film of tetraethyl orthosilicate by CVD.

7. A manufacturing method of a semiconductor device according to Claim 5, wherein:

said process for forming the oxide film is a process for forming a high-temperature oxide film by CVD.

8. A manufacturing method of a semiconductor device according to Claim 5, wherein:

said process for forming the oxide film includes a process for embedding an oxide film in said trench.

9. A method of manufacturing a semiconductor device substantially as either of the embodiments herein described with reference to the drawings.

10. A semiconductor device manufactured by the method of any of claims 1 to 9.

Application No: GB 0025595.0
Claims searched: 1-10

Examiner: Darren Handley
Date of search: 17 August 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1K (KGCCT, KGCW)

Int Cl (Ed.7): H01L 21/762

Other: Online: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	US6180490 B1	(VASSILIEV) - whole document relevant	
X	US 5786262 A	(JANG) - see column 3, line 55- column 4, line 38.	1-3, 5-7, 10
X	US 5943589 A	(OGUSHI) - see column 4, lines 17-59	1, 5

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.